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Appln. 2000-516470
Your Reference: 081513-31

(Translation)

Japanese Laid-Open Publication No. 11-168515

Laid-open publication date: June 22, 1999
Application number: 10-238440
Filing date: August 25, 1998
Priority claimed based upon Japanese Application No. 9-232557
Priority date: August 28, 1997
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Title of the Invention: Communication Apparatus

[Claims]

[Claim 1] A communication apparatus for performing high speed data transfer by a transmitter for outputting a digitally modulated signal to a transfer path and a receiver for demodulating the received signal into data, the communication apparatus including:

transfer speed control means for controlling a data transfer speed by an external control signal synchronized to a period of change of noise intensity.

[Claim 2] A communication apparatus for performing high speed data transfer by a transmitter for outputting a digitally modulated signal to a transfer path and a receiver for demodulating the received signal into data, wherein the receiver includes:

noise observation means for observing a time-wise change of noise intensity;

noise analysis means for analyzing a time-wise periodicity of the noise intensity observed by the noise observation means; and

transfer speed control means for controlling a data transfer speed in synchronization with a period of change of the noise intensity analyzed by the noise analysis means.

[Claim 3] A communication apparatus according to claim 1 r 2, wherein one period of the noise intensity change is divided into at least two time periods, and a processing speed of a modulator and a demodulator included in the transmitter and the receiver is switched in each divided time period in accordance with a signal to noise ratio in the receiver which is observed in each divided time period.

[Claim 4] A communication apparatus according to claim 1 or 2, wherein one period of the noise intensity change is divided into at least two time periods, and a coding ratio of an error correction code is switched in each divided time period.

[Claim 5] A communication apparatus according to any of claims 1 through 4, wherein the transmission path of the signal is a pair of twisted lines.

[Claim 6] A communication apparatus according to any of claims 1 through 4, wherein a plurality of carrier waves are used for transmitting data from the transmitter.

[Detailed Description of the Invention]
[0001]
[Field of the Invention] The present invention relates to a communicati n apparatus, and in particular to a communica-

tion apparatus for transferring a digital signal using a pair of twisted lines in which noise can be easily mixed.

[0002]
[Prior Art] A conventional communication apparatus always performs communication at a determined data transfer speed, or sets a usable transfer speed before the start of communication in consideration of the state of the transfer path and performs transmission at a determined transfer speed thereafter.

[0003]
[Problems to be Solved by the Invention] In a conventional communication apparatus, the upper limit of the data transfer speed is determined by an S/N ratio in a receiving circuit. When the level of noise mixed in the transfer path changes, the S/N ratio changes accordingly. In the conventional communication apparatus, communication is performed at the same transfer speed in a time slot when the S/N ratio is high and in a time slot when the S/N ratio is low. Therefore, in a communication apparatus performing communication at a predetermined transfer speed, when the S/N ratio changes time-wise, the number of transfer errors drastically increases in a time slot when the S/N ratio is low, which can disable communication. A communication apparatus in which the transfer speed can be set before the start of communication has the problem in that the transfer speed is determined in accordance with the time slot when the S/N ratio is low.

[0004] Especially in telephone subscribers' lines in Japan, high speed data transfer has the problem of the data trans-

fer speed being significantly reduced due to leakage noise from the existing "ping-pong ISDN" system.

[0005] Thus, a main objective of the present invention is to provide a communication apparatus for controlling a data transfer speed in synchronization with the period of change of noise intensity.

[0006]
[Means for Solving the Problems] The invention defined by claim 1 is directed to a communication apparatus for performing high speed data transfer by a transmitter for outputting a digitally modulated signal to a transfer path and a receiver for demodulating the received signal into data. The communication apparatus includes transfer speed control means for controlling a data transfer speed by an external control signal synchronized to a period of change of noise intensity.

[0007] The invention defined by claim 2 is directed to a communication apparatus for performing high speed data transfer by a transmitter for outputting a digitally modulated signal to a transfer path and a receiver for demodulating the received signal into data, wherein the receiver includes noise observation means for observing a time-wise change of noise intensity; noise analysis means for analyzing a time-wise periodicity of the noise intensity observed by the noise observation means; and transfer speed control means for controlling a data transfer speed in synchronization with a period of change of the noise intensity analyzed by the noise analysis means.

[0008] The invention defined by claim 3 is directed to a communication apparatus according to claim 1 or 2, wherein one period of the noise intensity change is divided into at least two time periods, and a processing speed of a modulator and a demodulator included in the transmitter and the receiver is switched in each divided time period in accordance with a signal to noise ratio in the receiver which is observed in each divided time period.

[0009] In the invention defined by claim 4, one period of the noise intensity change is divided into two at least two time periods, and a coding ratio of an error correction code in each divided time period.

[0010] In the invention defined by claim 5, the transmission path of the signal is a pair of twisted lines. In the invention defined by claim 6, a plurality of carrier waves are used for transmitting data from the transmitter.

[0011]
[Embodiments of the Invention] Figure 1 is a block diagram of an example of the present invention. In Figure 1, a modem 1 and a modem 2 are connected to each other via a pair of twisted lines, and digitally modulated signals are sent and received therebetween. The modem 1 includes a transmitting circuit 11 and a receiving circuit 12. The modem 2 includes a receiving circuit 21 and a transmitting circuit 22, and also includes a noise intensity monitor circuit 23 and a speed control signal generation circuit 24 built therein, which are features of the present invention. The noise intensity monitor circuit 23 observes a time-wise change of noise intensity based on the output from the receiving circuit 21, and analyzes the time-wise periodicity of the noise

intensity. An output from the noise intensity monitor circuit 23 is supplied to the speed control signal generation circuit 24, and thus a speed control signal for controlling the data transfer speed in synchronization with the period of change of the noise intensity is generated. The generated speed control signal is supplied to the transmitting circuit 22, and the transmitting circuit 11 and the receiving circuit in the modem 1.

[0012] Next, an operation of the invention will be described. The noise intensity monitor circuit 23 monitors a noise level based on the output from the receiving circuit 21. When the noise intensity monitor circuit 23 analyzes that the change of the noise level has time-wise periodicity, the speed control signal generation circuit 24 outputs a speed control signal for switching the transfer speed between a time slot when the S/N ratio is high and a time slot wh n the S/N ratio is low. Thus, a great amount of data can be transferred in the time slot when the S/N ratio is high.

[0013] Figure 2 is a timing diagram illustrating an operation of the communication apparatus shown in Figure 1. As shown in Figure 2, in the case of the "ping-pong ISDN" system, data is transferred downstream from a telephone station to a subscriber for 1.178 msec. Then, the next moment, data is transferred upstream from the subscriber to the telephone station for 1.178 msec. The method of transferring data with one period being divided into at least two time periods is referred to as burst transfer. There is an interval time period of 0.072 msec between the up-burst and the down-burst, and the up-burst and the down-burst are alternately transferred for a total period of 2.5 msec. From the viewpoint

of the station, signals to or from all the ISDN subscribers are sent and received synchronously.

[0014] An up-burst signal from an ISDN subscriber is mixed in a receiver of a non-ISDN subscriber's line as proximate leakage noise and thus reduces the S/N ratio. A down-burst signal from the station to an ISDN subscriber is mixed to a non-ISDN subscriber's line as distant leakage noise, but this is smaller than the proximate leakage noise from the up-burst signal. Therefore, it is preferable to find an optimum transfer speed with respect to each of the S/N ratio of an ISDN up-burst signal and the S/N ratio of an ISDN down-burst signal, and switch the transfer speed in synchronization with the switching of the ISDN burst signals.

[0015] The transfer signal can be switched by two methods. One is to switch the processing speed of the modulator and the demodulator. The other is to switch the coding ratio of an error correction code.

[0016] Figure 3 is a block diagram illustrating an example of switching the processing speed of the modulator and the demodulator. In Figure 3, the transmitting circuit 11 shown in Figure 1 includes an input buffer 111, a modulator 112, and a control circuit 113. The receiving circuit 21 includes a demodulator 211, an output buffer 212, and a control circuit 213. To the input buffer 111, input data is supplied. To the control circuit 113, a transfer speed c ntrol signal is supplied from the transfer speed control signal generation circuit 24. The control circuit 113 supplies a transmission signal control signal to the input buffer 111 based on the transfer speed control signal, and supplies a modulation speed control signal to the modulator 112. The

control circuit 214 in the receiving circuit 21 supplies a demodulation speed control signal to the demodulator 211 upon receiving the transfer speed control signal, and supplies a receiving speed control signal to the output buffer 212.

[0017] In this example, the transmission speed of the input buffer 111 of the transmitting circuit 11 and the modulation speed of the modulator 112 of the transmitting circuit 11 are controlled in accordance with the transfer speed control signal. The demodulation speed of the demodulator 211 of the receiving circuit 21 and the receiving speed of the output buffer 212 of the receiving circuit 21 are controlled also upon receiving the transfer speed control signal. In this way, the data transfer speed can be controlled in synchronization with the period of change of the noise intensity. Thus, an optimum transfer speed can be set.

[0018] Figure 4 is a block diagram illustrating another example of switching the processing speed of the modulator and the demodulator. In Figure 4, the transmitting circuit 11 has a similar structure to that in the example shown in Figure 3. The receiving circuit 21 further includes a synchronization extraction circuit 218. In the example shown in Figure 3, the demodulation speed control signal and the receiving speed control signal are output upon receiving an external transfer speed control signal. By contrast, in th example shown in Figure 4, based on the demodulation output of the demodulator 211, the synchronization extraction circuit 218 outputs the demodulation speed control signal and the receiving speed control signal in synchronization with the period of change of the noise intensity.

[0019] Figure 5 is a block diagram illustrating an example of switching the coding ratio of an error correction code. In Figure 5, the transmitting circuit 11 includes a convolution code circuit 114 between the input buffer 111 and the modulator 112. A control circuit 115 supplies a reading speed control signal to the input buffer 111 and supplies a coding ratio control signal to the convolution code circuit 114 both in accordance with the transfer speed control signal. The receiving circuit 21 includes a Viterbi decoding circuit 214 between the demodulator 211 and the output buffer 212. A control circuit 216 supplies a decoding mode control signal to the Viterbi decoding circuit 214 in accordance with the transfer speed control signal.

[0020] In this example, in the transmitting circuit 11, a punctured coding technology is used by which the convolution code circuit 114 deletes a symbol from a convolution code by a coding restraining control signal, thereby improving the coding ratio. The receiving circuit 21 also performs a demodulation operation corresponding to the coding ratio of the receiving data using the Viterbi decoding circuit 214.

[0021] Figure 6 is a block diagram of still another example of the present invention. This example uses a pair of twisted lines as a transfer path, and includes a station modem 10 and a subscriber modem 20. The station modem 10 and the subscriber modem 20 are each a combination of the transmitting circuit and the receiving circuit shown in Figure 4. Namely, the station modem 10 includes an input buffer 111, a modulator 112 and a communication control circuit 113 acting as the transmitting circuit, and also includes a demodulator 215, an output buffer 216, and a reception control circuit 217 acting as the receiving circuit. The station modem 10

further includes a hybrid circuit 6 for connecting the modulator 112 and the demodulator 215 to a pair of twisted lines 5 as the transfer path.

[0022] The subscriber modem 20 includes an input buffer 114, a modulator 115, and a transmission control circuit 116 as the transmitting circuit, and a demodulator 211, an output buffer 212, a synchronization extraction circuit 218, and a reception control circuit 213 as the receiving circuit. The subscriber modem 20 further includes a hybrid circuit 7 for connecting the modulator 115 and the demodulator 211 to the pair of twisted lines 5.

[0023] The operation of the transmitting and receiving circuits in each of the station modem 10 and the subscriber modem 20 is the same as that shown in Figure 4. Data can be sent and received bidirectionally. The station modem 10 and the subscriber modem 20 may be of a symmetric type in which the transfer speeds of the two are the same or of an asymmetric type in which the transfer speed of one is higher than that of the other.

[0024] Figure 7 is a block diagram illustrating a modulator and a demodulator realized by a plurality of carrier waves to which the present invention is applicable. In Figure 7, (a) represents the modulator, and (b) represents the demodulator.

[0025] In Figure 7, input data is input to a constellation encoder 31 and symbol-arranged so as to be quadrature-modulated. In quadrature-modulation, data is arranged two-dimensionally by sine waves and cosine waves, and data bits ar assigned to each carrier wave in accordance with the S/N

ratio. A great number of bits are assigned two-dimensionally to at least carrier waves having a high S/N ratio. The symbol-arranged data is supplied to an IDFT 32 to be inverse-Fourier-transformed. Parallel data is transformed to serial data by a P/S transformer 33. The serial data is converted into an analog signal by a DAC 34, and the modulated signal is output from a driver 35.

[0026] In the demodulator shown as (b) in Figure 7, an input signal is supplied to a receiver 41 and converted into a digital signal by an ADC 42. The serial signal is transformed by an S/P transformer 43 into a parallel signal, which is Fourier-transformed by a DFT 44. A constellation decoder 45 performs the inverse processing to that of the constellation encoder 31. Thus, data is output.

[0027] Figure 8 shows an example of an arrangement of a plurality of carrier waves provided by the modulator and the demodulator shown in Figure 7. In this example, a plurality of carrier waves are arranged within a frequency range of 30 kHz to 1104 kHz at a frequency interval of 3125 kHz. A modulator and demodulator realized by such a plurality of carrier waves can be used instead of the modulator and the demodulator shown in Figures 3 through 5.

[0028]
[Effect of the Invention] As described above, according to the present invention, a time-wise change of noise intensity is observed on the receiving side, and the time-wise periodicity of the noise intensity is analyzed so that the data transfer speed is controlled. Therefore, a large amount of data can be sent in a time slot when the S/N ratio is high.

[Brief Description of the Drawings]
[Figure 1] A block diagram illustrating an example of the present invention.

[Figure 2] A timing diagram illustrating an operation of the example shown in Figure 1.

[Figure 3] A block diagram illustrating an example of switching the processing speed of a modulator and a demodulator.

[Figure 4] A block diagram illustrating an example of switching the processing speed of a modulator and a demodulator.

[Figure 5] A block diagram illustrating an example of switching the coding ratio of an error correction code.

[Figure 6] A block diagram illustrating another example of the present invention.

[Figure 7] A block diagram illustrating a modulator and a demodulator realized by a plurality of carrier waves to which the present invention is applicable.

[Figure 8] A diagram showing an arrangement of a plurality of carrier waves of the modulator and the demodulator shown in Figure 4.

[Description of the Reference Numerals]
1, 2 Modem
5 Pair of twisted lines
6, 7 Hybrid circuit

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11, 22 Transmitting circuit
12, 21 Receiving circuit
23 Noise intensity monitor circuit
24 Speed control signal generation circuit
31 Constellation encoder
32 IDFT
33 P/S
34 DAC
35 Driver
41 Receiver
42 ADC
43 S/P
44 DFT
45 Constellation decoder
111, 114 Input buffer
112, 115 Modulator
113, 115, 213, 215 Control circuit
114 Convolution code circuit
211, 215 Demodulator
212, 216 Output buffer
214 Viterbi decoding circuit
218 Synchronization extraction circuit

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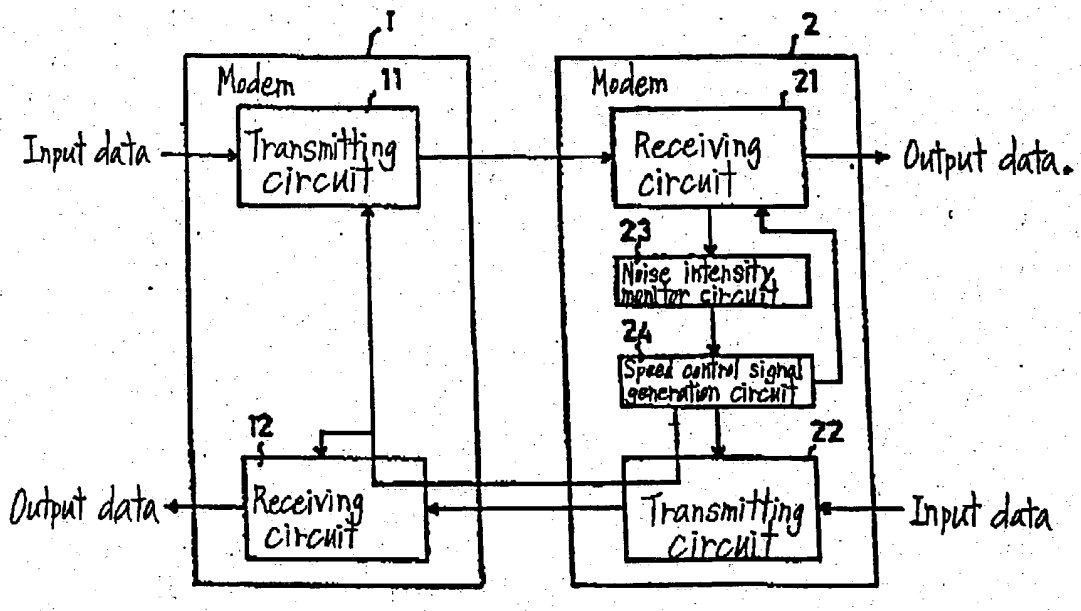
(Fig. 1)



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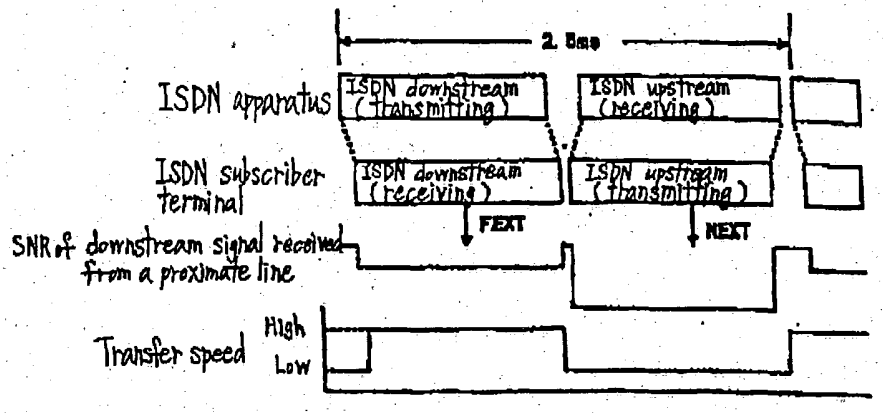
[Fig. 2]



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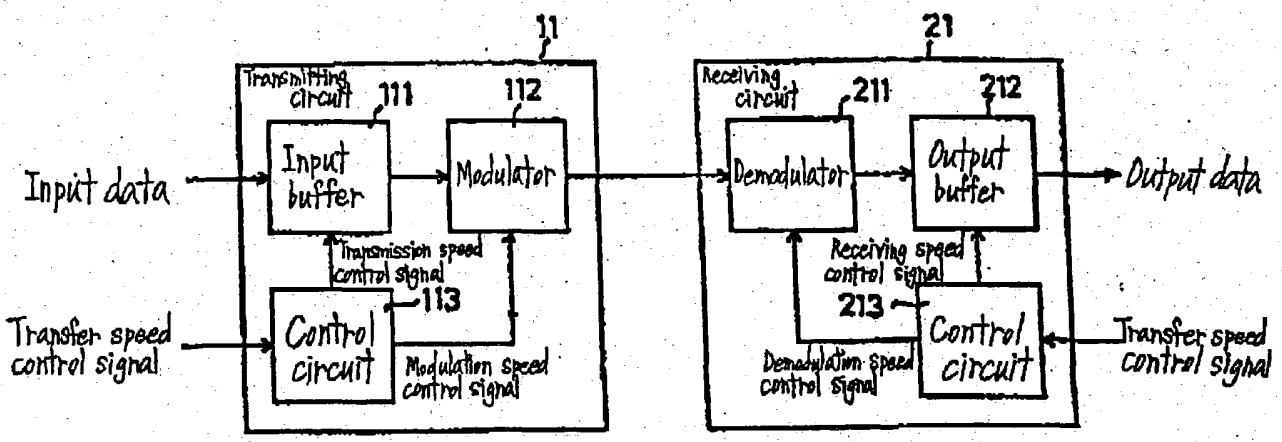
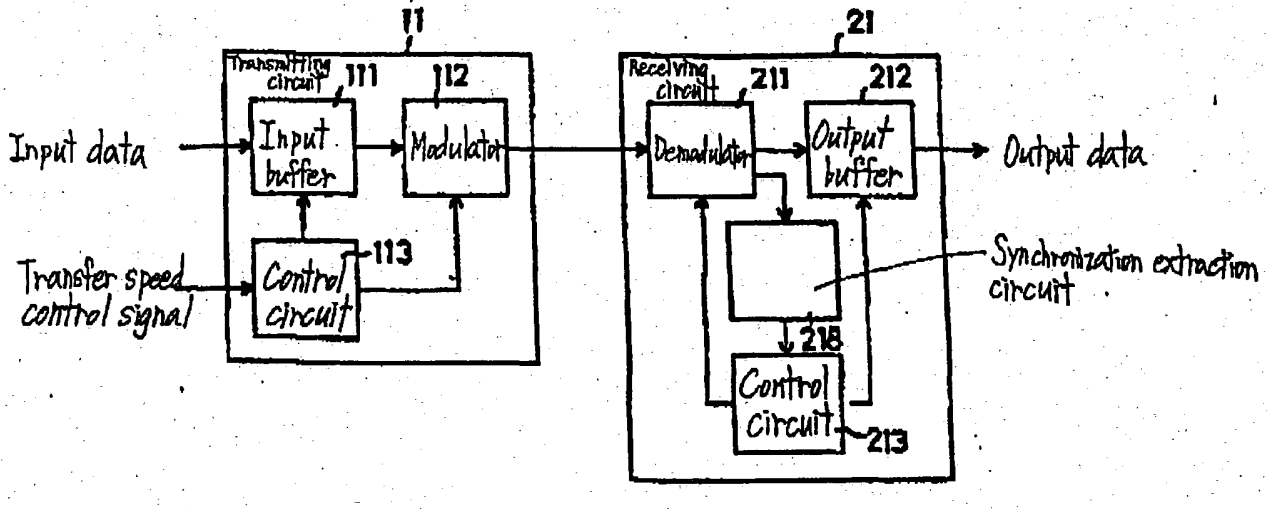
[Fig. 3]



[Fig. 4]



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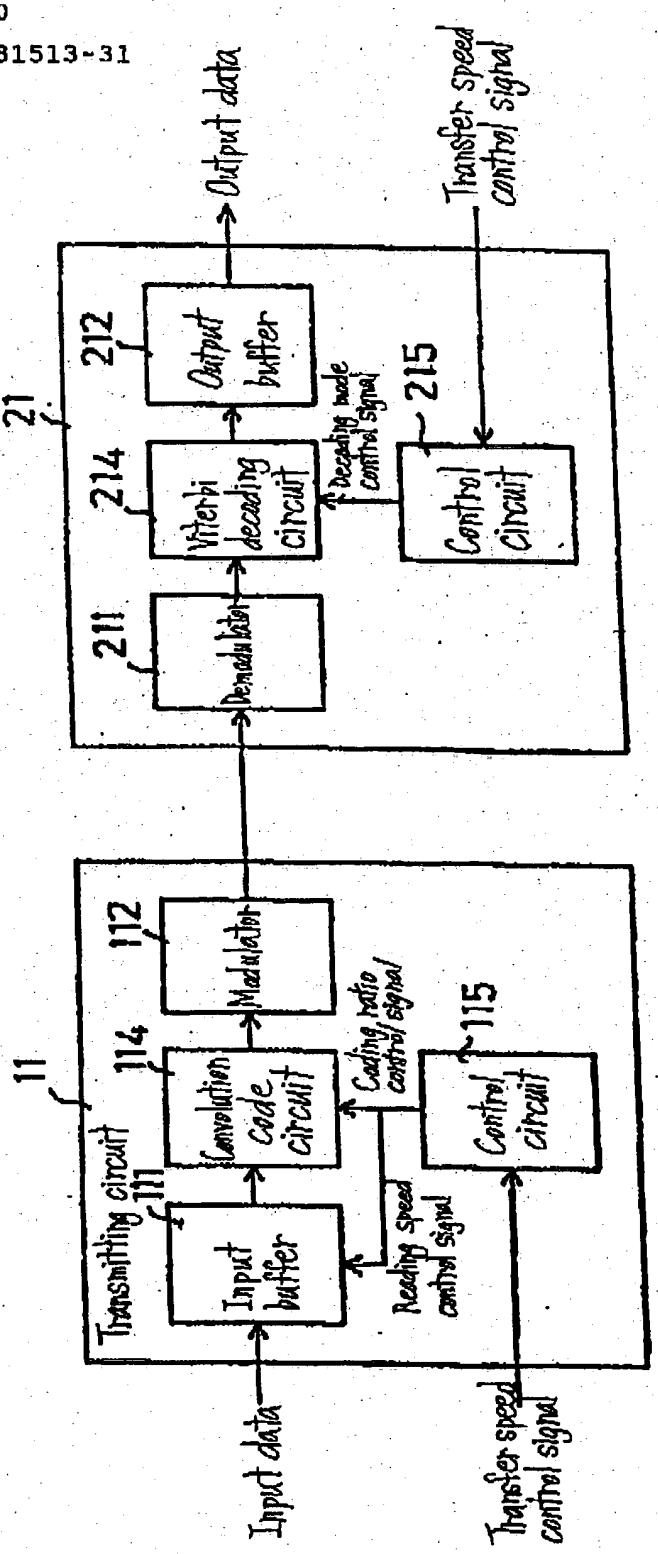
[Fig.5]



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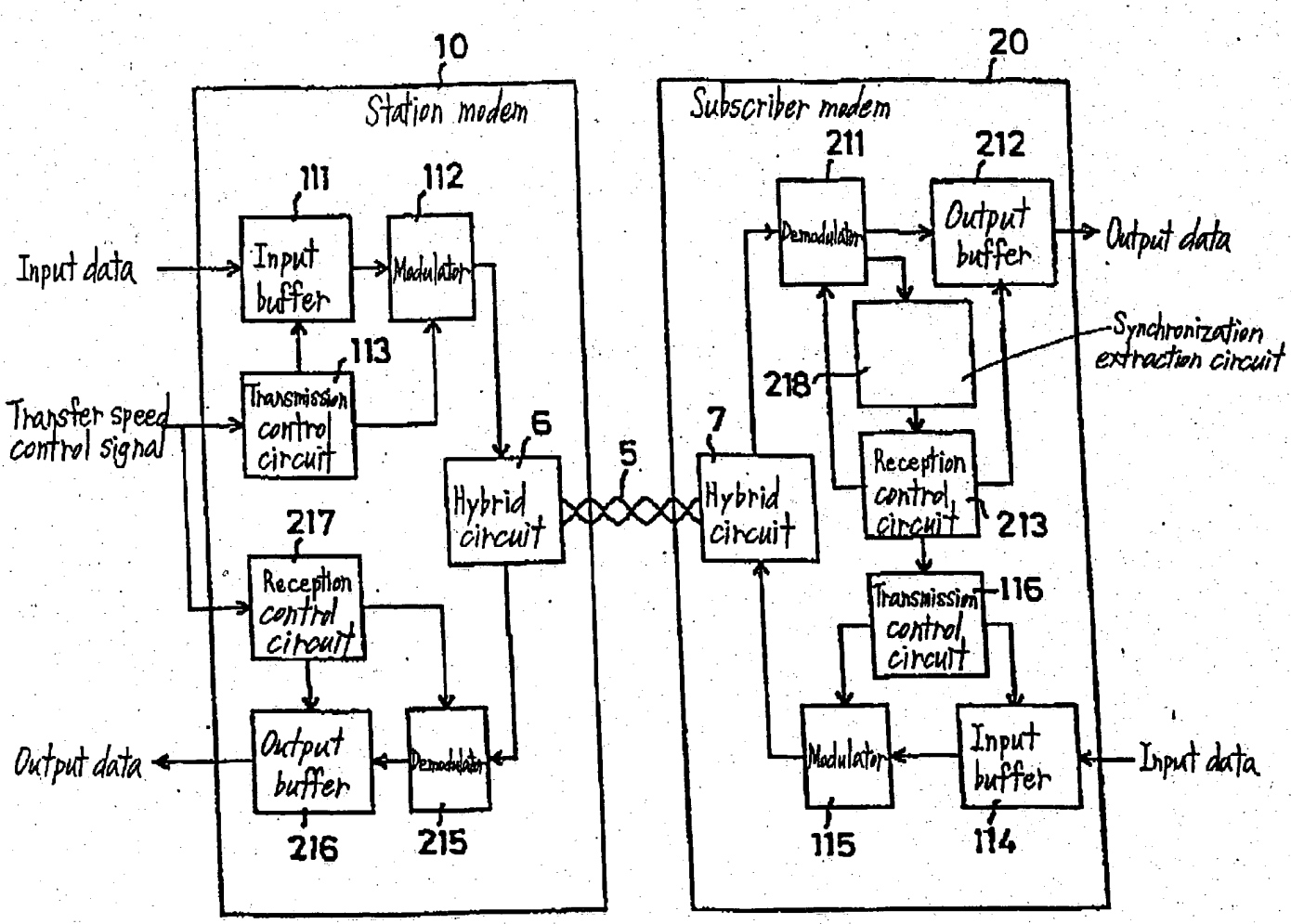
[Fig. 6]



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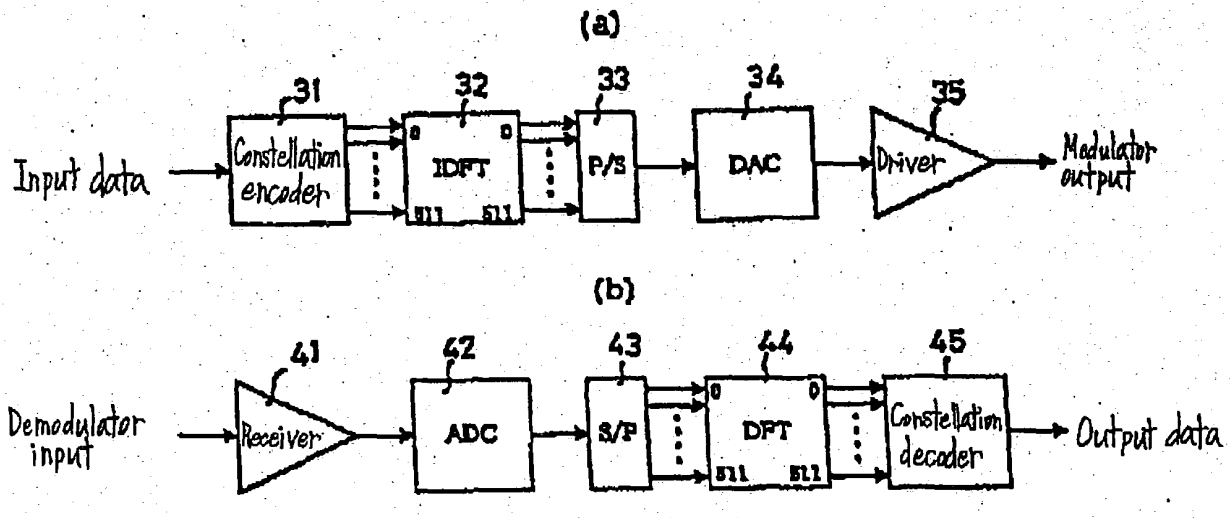
(Fig. 7)



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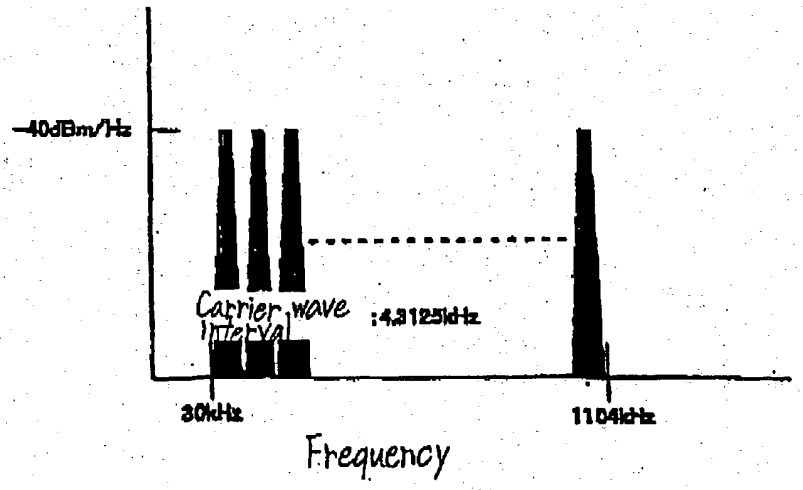
[Fig. 8]



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[Abstract]
[Problems] To control the data transfer speed in synchronization with a period of change of noise intensity.

[Means for Solving the Problems] A noise intensity monitor circuit 23 observes a time-wise change of the noise intensity based on an output from a receiving circuit 24. A speed control signal generation circuit 24 analyzes the periodicity of the time-wise change and thus generates a speed control signal so as to control a data transfer speed of transmitting circuits 11 and 22 and a receiving circuit 12. Thus, a great amount of data can be sent in a time slot when the S/N ratio is high.